NectarCAM TC Status

NectarCAM Progress Meeting
April 6th 2021

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DT Status

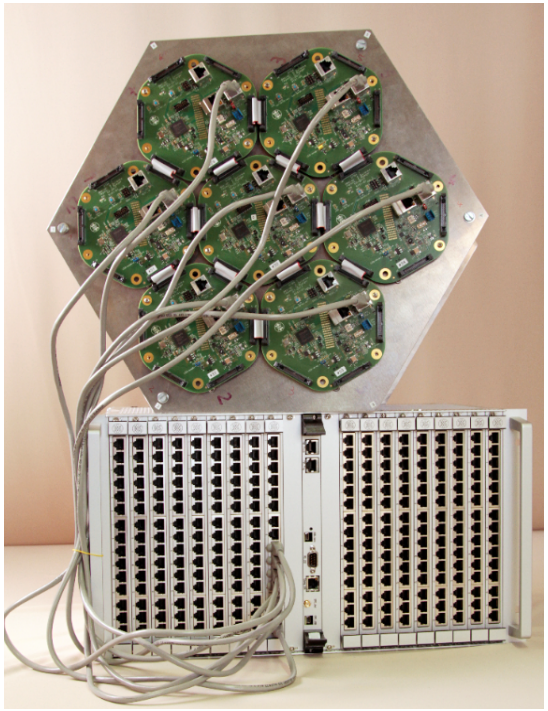
Changing the Distributed Clock, 50MHz -> 66MHz

- Motivated by the FEB team, to run the FEBs globally synchronized
  - Using the DTB signal EXTXCLK_P/N
- The firmware for the three different modules in the digital trigger schema got adapted (DTB, CTDB, L2CB)
  - Refurbished the DESY test setup (1 CTDB only)
  - Issue: it was not possible to program the L2CB via JTAG anymore
    - Caused by the migration of the Xilinx development system ISE from Windows 7 to Windows 10 + USB driver issue only visible at (my) fast PC
    - Is now, after 1.5 days of investigations, understood
    - C155 has to get removed
- New firmware available:

  DTB4,

  CTDB2,

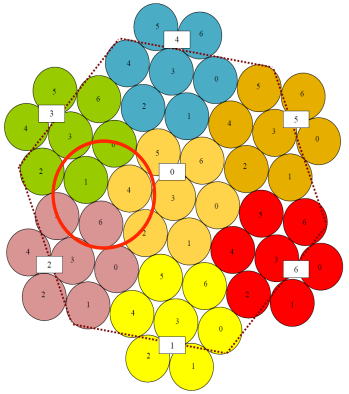
  L2CB1,

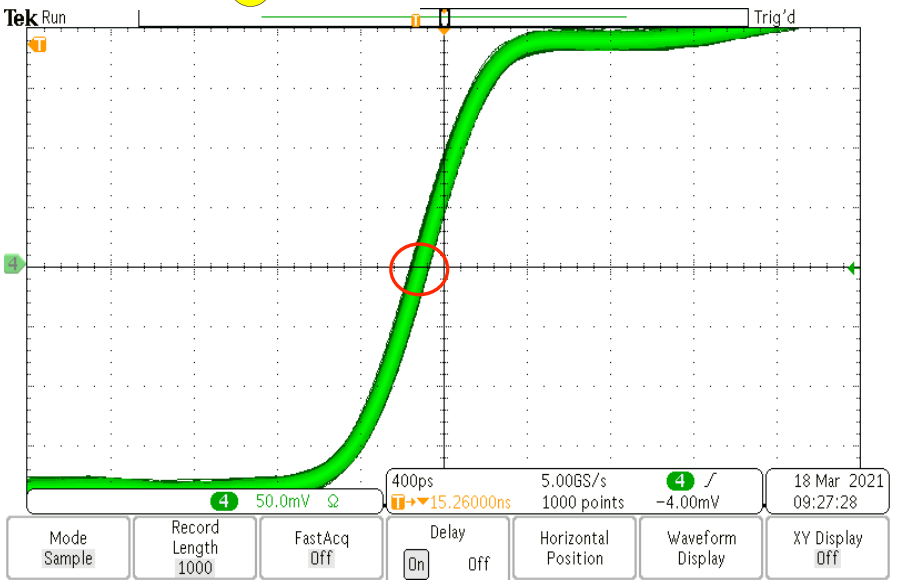


DT Status

Testing the 66MHz Firmware Versions

- Tested some basic functionality (only):
  - Clock and PPS encoding / decoding
  - L0 delay adjustment
  - 3NN trigger between three DTBs
  - L1 delay adjustment (L2CB)
  - L2 trigger (L1A) generation
  - FEB-clock (EXTCLK_P/N) cycle to cycle jitter
    - Scope, diff. probe, trigger delayed by one clock cycle
    - 80ps after 20 minutes in infinite persistance mode

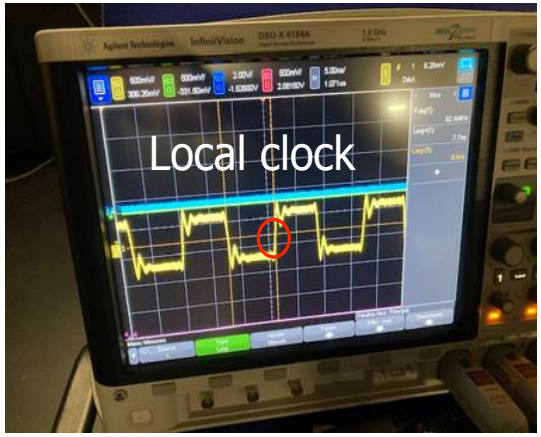


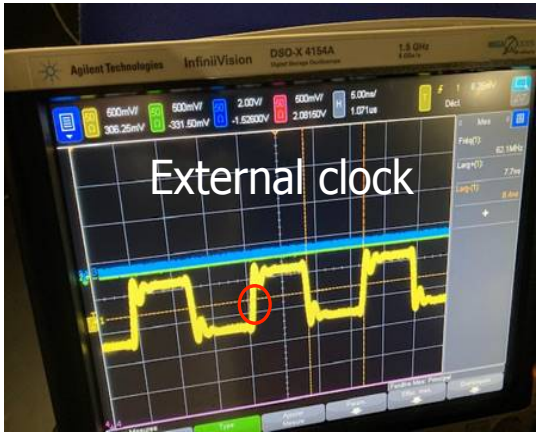


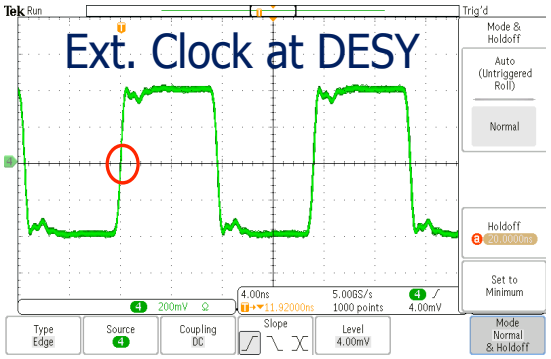
DT Status

Testing the 66MHz with the latest FEBs at Saclay

- See the first two pictures below, Francois might comment …
- the comparison of the local clock with the external clock using a scope showed different waveforms:







- Got interpreted as jitter of the external clock, but if so, I would expect a sharp edge at the trigger position, not a homogeneously smeared waveform
- My explanation, it is just a grounding issue
- Not visible at the DESY test setup, using a diff. probe

DT Status

Future Plans

- QM parts delivered
- Sending a spare L2CB1 to Saclay and assembly of 10 additional CTDBs
  - Parts procurement has started
  - Presently hard to get parts, e.g. Xilinx FPGAs
  - Probably have to order at a broker, like 4Source
- Recruit a successor
  - I will be retired at 27th of March 2023
  - Esp. for firmware development / improvement / bug fixing
  - A good candidate do exist, still have to ask him …
- To be considered by the management (David Berge at DESY), the financing of the digital trigger!
  - As I remember, DESY agreed to pay for the QM only (I might be not up to date)
- CDMR related
  - Although a detailed plan was made, zero progress so far, sorry for this!
  - For my opinion the available technical documents are sufficient for replication / debugging (by an engineer)
  - I agree, the documentation can get improved
  - Due to my present situation I hesitate to make further / update the existing plan

DTS docs pending update

Topic	Update done
DTB f/w architecture	2021-02-28
CTDB f/w architecture	2021-02-28
L2CB f/w architecture	2021-03-07
L2CB s/w architecture	2021-03-07
L2CB L2Crate ICD	2021-03-14
DTB CTDB ICD	2021-03-14
L2 Crate Mechanics ICD	2021-03-14
L2Crate PSB ICD	2021-03-21
L2CB Slow Control ICD	2021-03-21
DTS Performance verification	2021-03-21
DTS QC procedure for production	2021-03-31
DTB user manual	2021-03-31
CTDB user manual	2021-03-31
L2CB user manual	2021-03-31

TIB Hardware

2 new TIBs v5 to be received next week

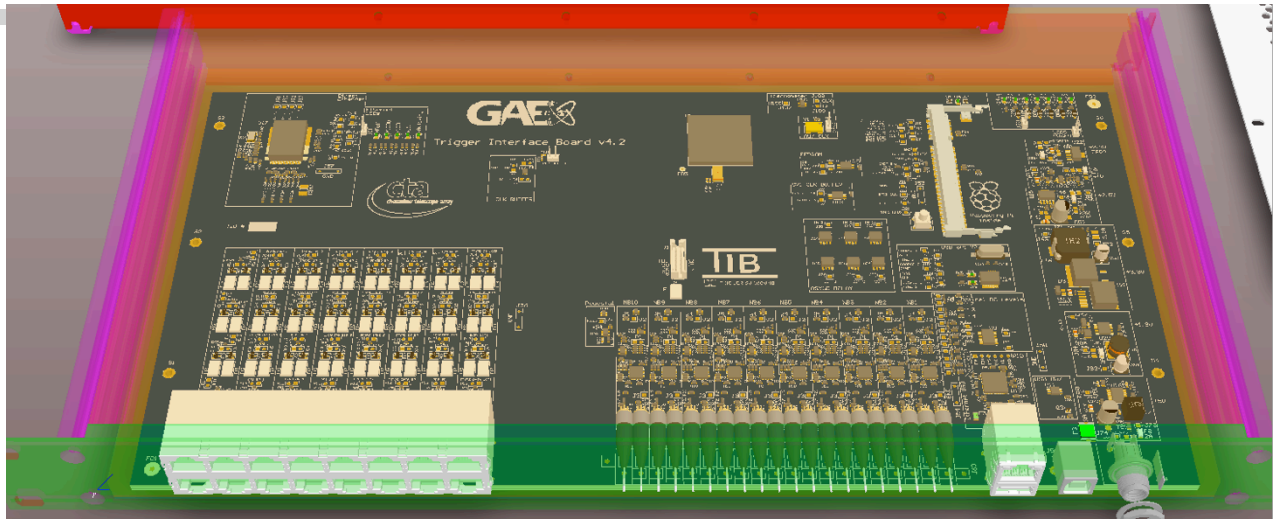
TIB v5 solves several issues:

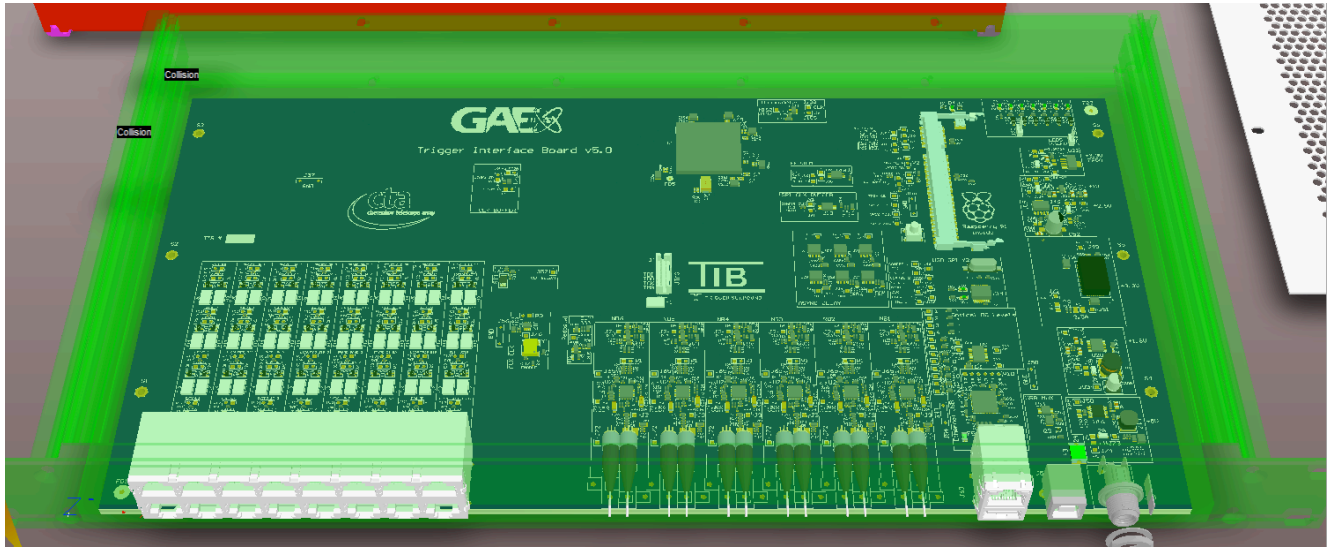
- Reduction of optical channels from 10 to 6.
- Great reduction of crosstalk between optical channels expected. This is useful not only for stereo trigger, but also for calibration trigger or any other optical trigger signal.
- Internal clock available and selectable by slow control. This makes possible (if needed for emergency local operation, not recommended) for the TIB to work without UCTS.
- Obsolescence avoided by replacing some regulators in the power supplies.

More units of TIB v5 to be manufactured during 2021-22:

- Once a TIBv5 for LST1 is produced (~July 2021) a TIBv4 can be sent to Saclay for T66, while another one remains in the QM
- Six TIB v5 (5 for MST-1-5-N + 1 spare) by mid 2022 (funding still unclear)

TIB Hardware





TIB Firmware

A new firmware release (v3) for TIB v4 and v4.2 is available since January. It has been deployed at LST and it is being used successfully.

- It allows to switch on and off the replication and reception to/from optical channels independently, reducing crosstalk.
- Counters improved. Trigger input counters count asynchronous edges instead of shaped pulses. Readable from state 0.
- Trigger type assignation improved, considering trigger inputs appearing in a 20 ns time window.
- Trigger type assignation tested in depth. Glitch free.
  - Always Camera + Busy = Collected
  - Last event number in TIB slow control = last event number in TIB data for EVB = last event number in UCTS data.
  - Last Busy trigger in TIB slow control = last Busy trigger in UCTS data

TIB Firmware: double-pulse test

- 1 kHz of 200 ns wide L1 double pulses
- UCM setup (~1 us simulating camera busy)

Separation	L1 rate	Collected	Camera	Busy
200 ns	999	999	999	0
204 ns	1998	999	999	0
382 ns	1998	999	999	0
383 ns	1998	1014	999	15
387 ns	1998	1998	999	999
1205 ns	1998	1999	999	999
1210 ns	1998	1998	1130	868
1215 ns	1998	1998	1998	0

TIB Firmware

- Special shaping for trigger pulses with exponential decay.
- Improved reliability of the busy handler.
- Firmware ready for absolute time-stamping at TIB. A GPIO is rised to warn the RPi about the first PPS leading edge.
- New DebugVector datapoint available for easier debugging.
- New firmware datapoint containing firmware version.
- Busy monitor upgraded for real measure of dead time. Requires software update.
- Quality improved: Many firmware simplifications and better timing constraints.

A lot of improvements as a result of 1.5 years of tests!

TIB Firmware: Known Issues

- Polarity of the SPI link with the UCTS. Currently CPOL = 1 and CPHA = 1. Ready to change to 0 in the next UCTS firmware update.
- Repeated data for the same event trigger pulse: Sometimes a camera trigger pulse generates two data patterns which are sent to the EVB. The first one contains the real trigger type. The second one has the same event number, but trigger type 0 (or 128 if we consider the Busy bit in bit 7). This can be fixed by software at TIB &/or EVB &/or Analysis.
- Error bursts: Wrong data from a certain bit in the 50 event data packet sent to the EVB. It is related with the SPI link between FPGA and Raspberry Pi. This can be fixed by software.

TIB Software: OPC-UA

There are several new features ready. Tested in the laboratory, but not yet at LST or NectarCAM:

- More fine delay external delay adjustment between 3525 and 3588
- New TIB busy time datapoint included.
- New datapoint with power supply status included.
- DebugVector datapoint included.
- New datapoint with firmware version included.

TIB Software: EVB Comm.

A new software version, able to provide absolute time-stamping to the EVB is ready. Current one only provides time-tags.

This new feature is difficult to deploy, because it requires strong coordination with EVB.

The possibility to correct bursts of triggers with wrong information in this software is under study.

UCTS Hardware

- Hardware Status
  - **TiCkS board**:
    - 10 boards in a pre-series produced → ready for the QM and Pathfinder.
    - 10 additional boards produced and waiting to be stuffed
  - **Rack Box**:
    - Working on the new front-panel both for LST and for the NectarCAM QM.
    - Due to occupation of the mechanics workshop, it will by ready in April for the QM.
    - First to check that all is fitting together for LST; then produce another one for NectarCAM.
  - **Remote Programming Board:**
    - Completely independent of the TiCkS itself,
    - Second prototype (hopefully final version!) being produced, expecting to arrive by the end of the week.
    - Need to be further debugged, after which we can hope that it works (if the LAN problems are solved) → not ready for QM, but ready for Pathfinder

UCTS Software

A new OPC-UA plugin including new features has been developed:

- Up time
- GetSNMPSwVersion
- GetSNMPTimeTAI
- GetSNMPPortStatus
- Temperature

Those data points were developed for monitoring. They use the UCTS capability to answer to SNMP requests. The UCTS needs to be configured, with the IP directions, before answering to any SNMP request.

UCTS Software

- CDTS-Server software
  - Software receiving x24 UCTS timestamp-packets and delivering x1 UCTS timestamps to EVB
  - Officially a camera element
  - v0.6 running automatically at LST1

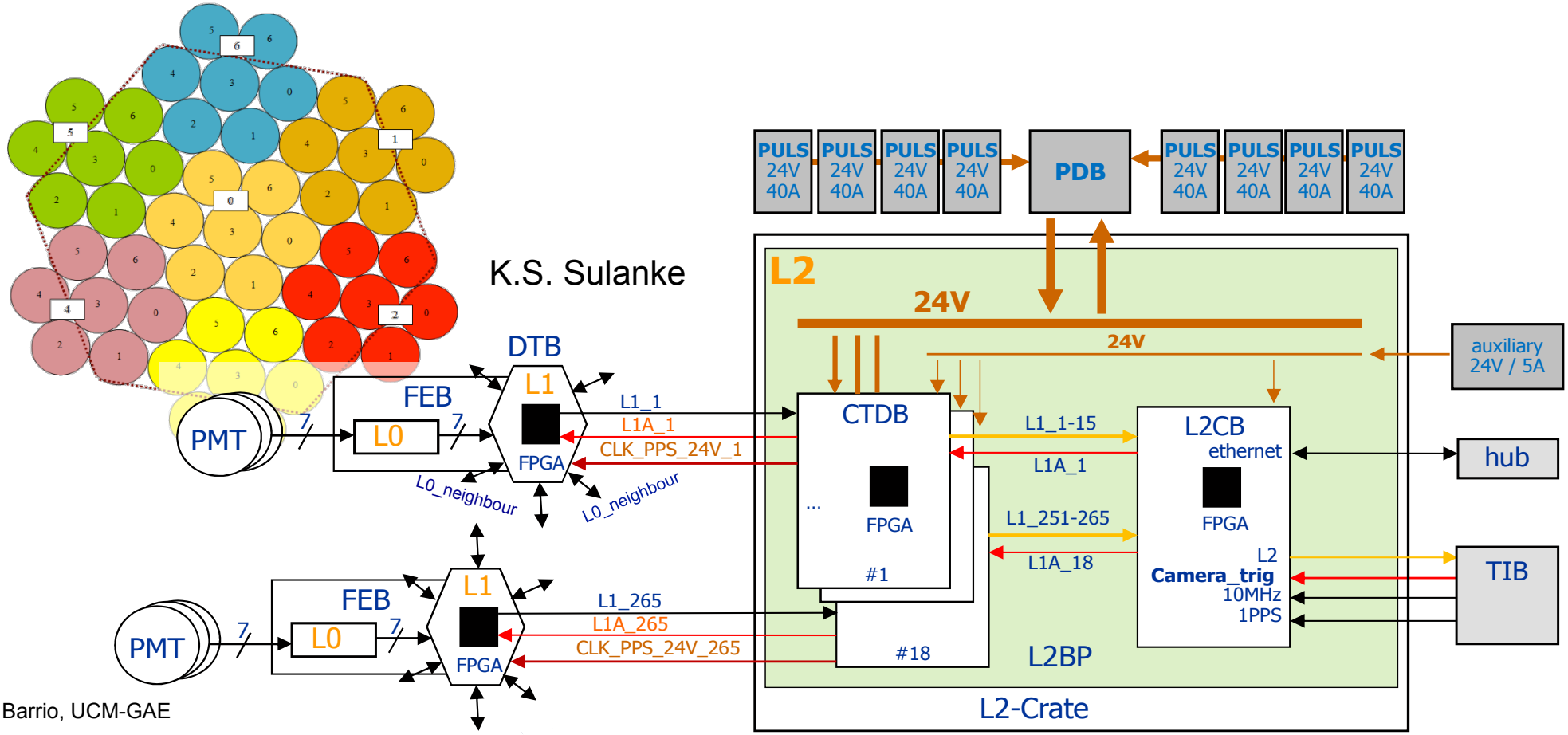
CDMR

- Coordination:
  - 2 document pending update (after panel feedback in January):
    - TC system design summary, CIDL.
  - No specific TC document in the CDMR high-priority action-list. Still, TC input for the high-priority action-list might be needed.
  - RM ticket feed-back after CDMR meeting not checked yet. In any case, all normal-priority tickets to be completed before first acceptance review ?!
- DTS:
  - 14 documents pending update
- TIB:
  - No document pending update
- UCTS:
  - 1 document pending update:
    - UCTS User Manual

Backup

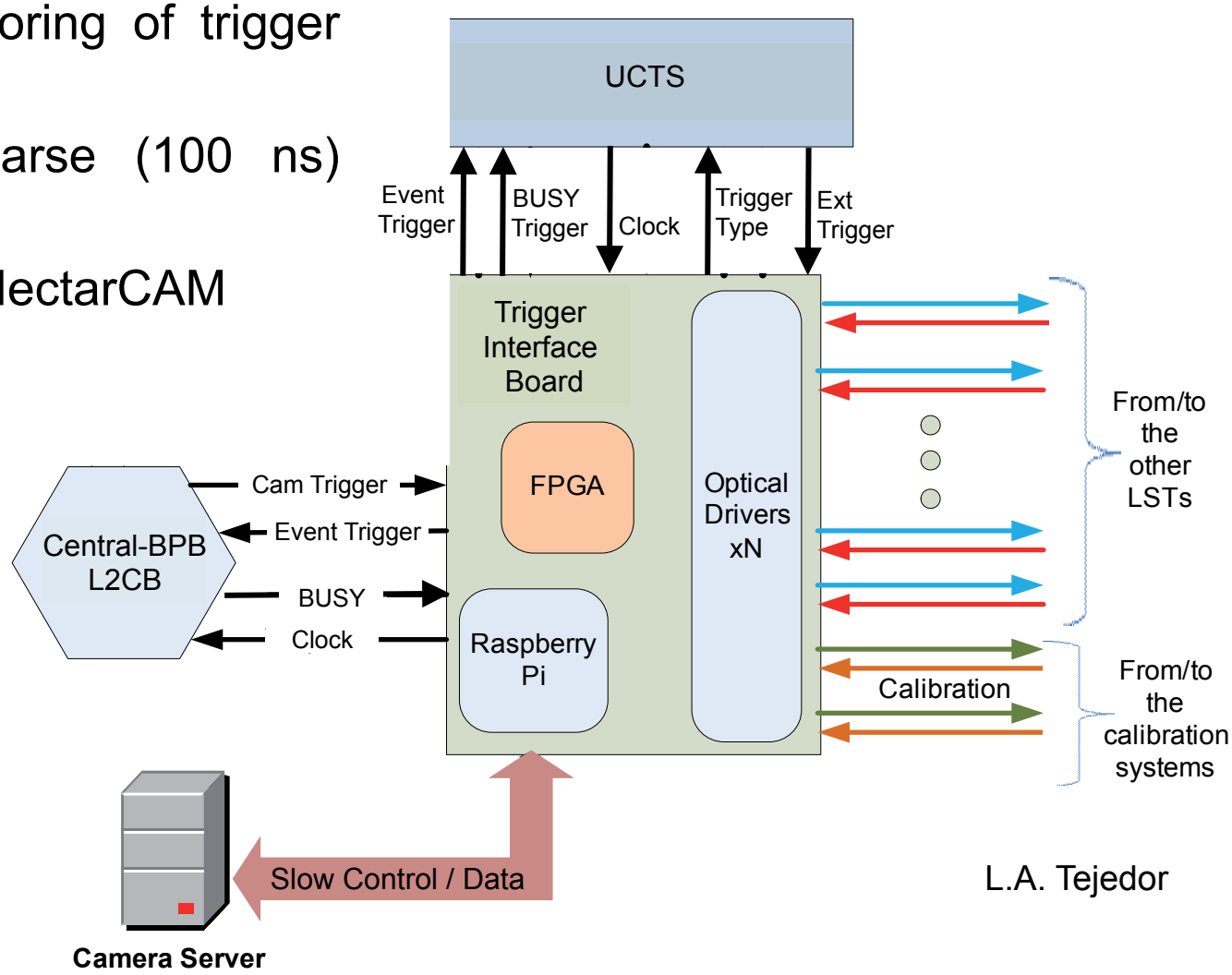
DT Status

- Digital Trigger System:
  - Trigger Decision: L0 ASICs @ FEE, L1 @ DTB, L2 @ L2-Crate
  - Trigger & Clock Distribution: CTDBs @ L2-Crate, DTBs
  - Power distribution/control to FEB/FPM: 24 V via CTDBs @ L2-Crate



TIB Status

- Trigger Interface Board:
  - Management & monitoring of trigger and clock signals
  - Trigger type and coarse (100 ns) timestamp of events
  - Common to LST and NectarCAM



UCTS Status

- Unified Clock distrib. & Trigger time-Stamping board:
  - Camera White Rabbit node for Clock Distrib. & Trigger time-Stamp (CDTS)
  - Ticks-UCTS designed by APC, common to LST and NectarCAM
  - Delivery of clock signals for camera synch & generation of 1-ns timestamps