Camera Design for SC Telescope

Jim Buckley for the CTA-US Camera group

Washington University
St. Louis, Missouri, U.S.A.

CTA-US Meeting
SLAC, Feb 2012

SC Camera WG

- Aurelien Bouvier (UCSC)
- Jim Buckley (WU) (Backplane,Trig)
- Karen Byrum (ANL)
- Stefan Funk (SLAC) (FEE TARGET)
- David Hanna (McGill)
- Brian Humensky (Columbia)
- David Kieda (UU)
- Henric Krawczynski (WU)
- Frank Krennrich (ISU) (Array Trigger)
- Phil Moore (WU)
- Reshmi Mukherjee (Barnard)
- Nepomuk Otte (Georgia Tech)
- John Quinn (UCSD)
- Leonid Sapozhnikov (SLAC)
- Martin Schroedter (SAO)
- Hiro Tajima (SLAC)
- Justin Vandenbroucke (SLAC)
- Bob Wagner (ANL)
- Scott Wakely (UC) (Camera Mechanics)
- Amanda Weinstein (ISU)
- David Williams (UCSC) (Photodetectors)

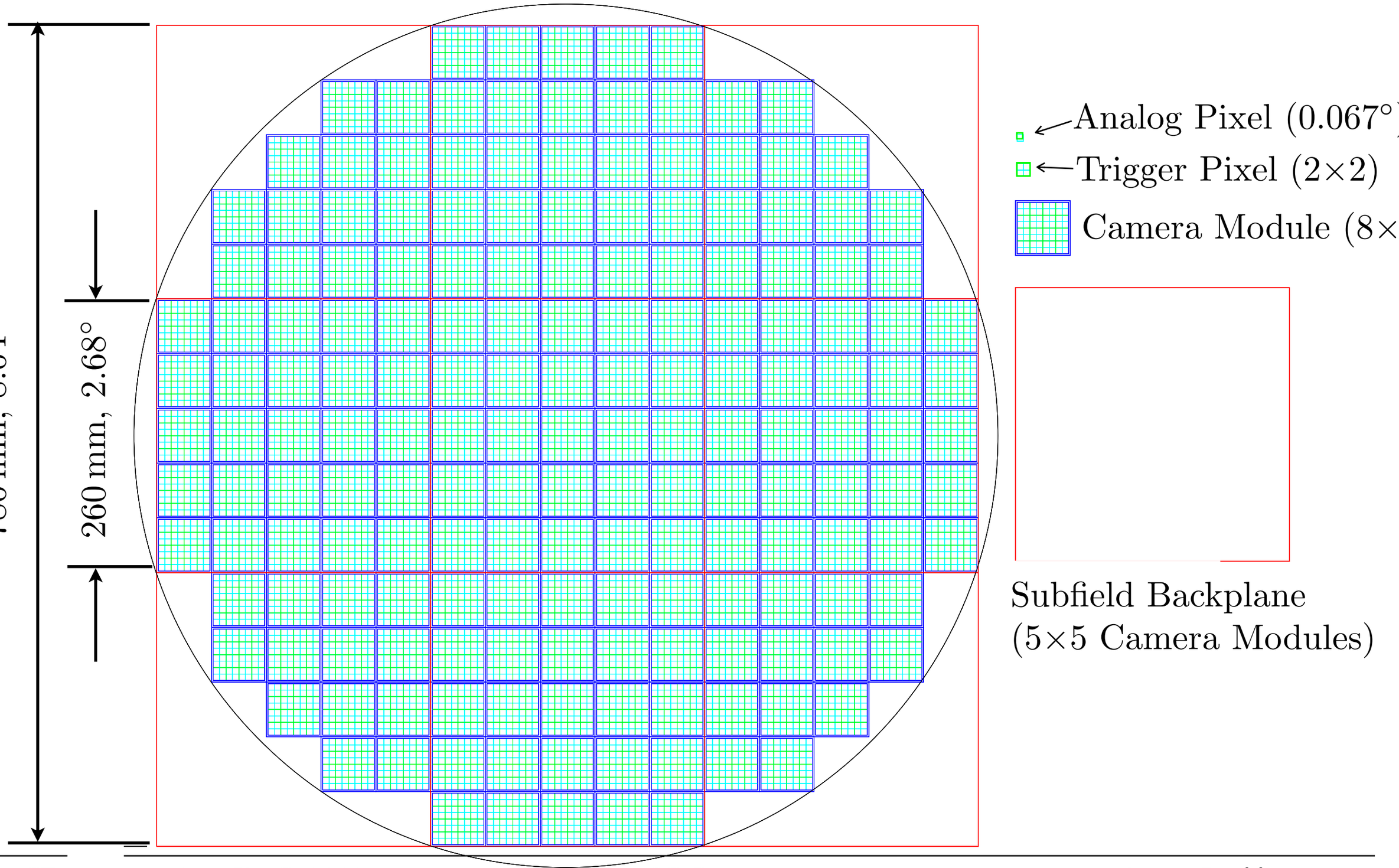
Work Plan

- Still no Federal Funding, but we need to continue to design the Camera!
- Write PTDR Document
- Write Specifications Document (this will be evolving)
- Define interfaces in a series of ICDs
- Provide detailed lists of components for beginning of budget estimate (start with part numbers, for uniform costing - quantity discounts)
- Come up with a list of questions for Simulations Group. Generate attached documents motivating specifications.

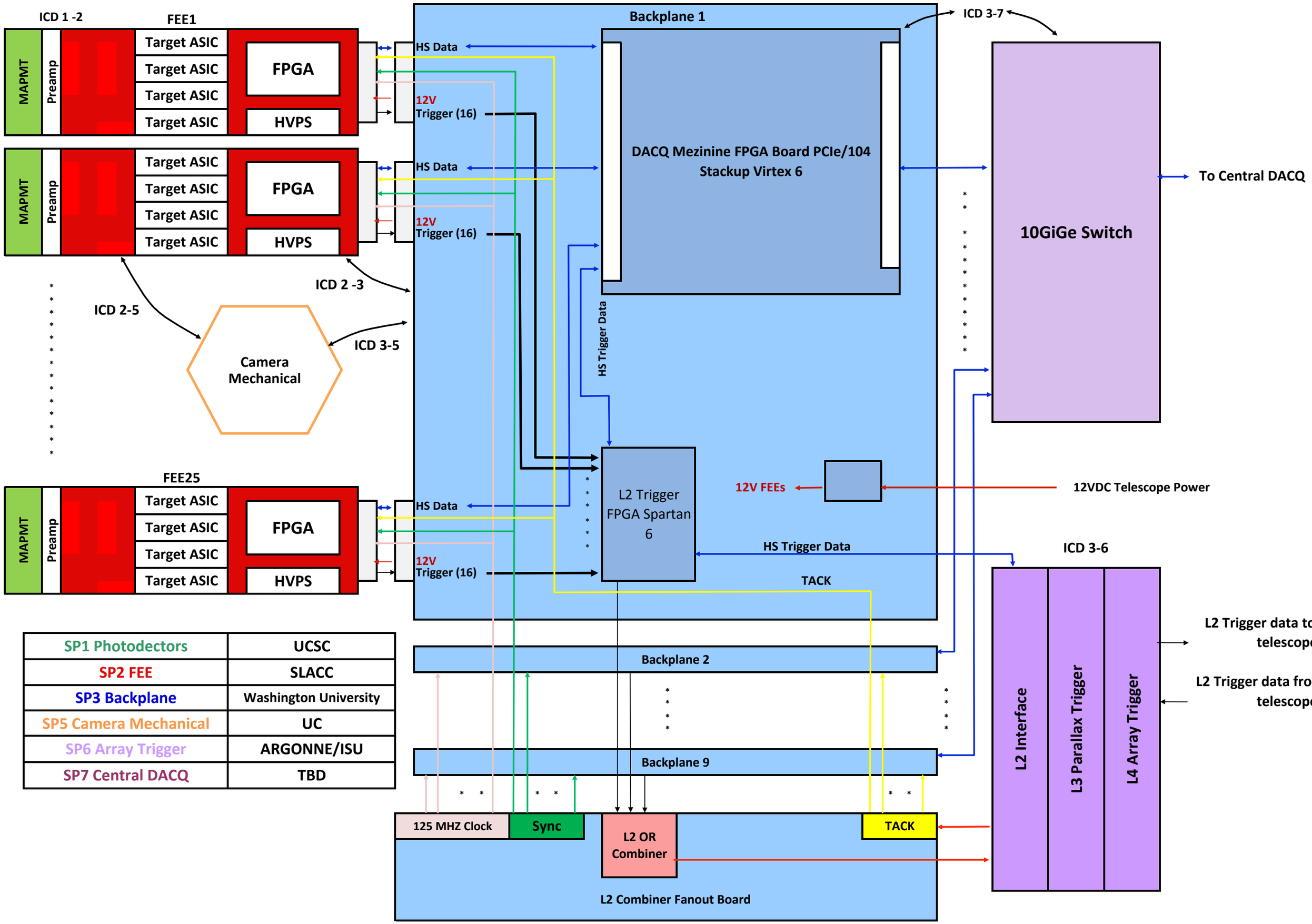
Working Group Structure

- **SP1 Photodetectors** (UCSC): MAPMTs and SiPMs, thermal/hermetic system design, testing, characterization and calibration, vendor selection.
  - Participants: UCSC, Georgia Tech, Barnard, ANL
- **SP2 Front-end electronic**s (SLAC): TARGET ASIC, front-end boards with A/D, L1 discriminators, HV modules
  - Participants: SLAC, UC, Hawaii, (Preamp ASIC at WU)
- **SP3 Camera backplane** (WU): DAQ from FEE, L2 (pattern trigger), front-end CPUs and ethernet output, current monitor, HV control,
  - Participants: WU, UC, ISU
- **SP4 Telescope DAQ** (TBD): Telescope DACQ computers and software, realtime data processing/compression
  - Participants: SLAC
- **SP5 Camera-mechanical, integration** (UC): Design of mechanical systems for FEE, camera positioning, shutter design, cooling, monitoring, slow control, integration of all subsystems
  - Participants: UC, UU, UD, GT
- **SP6 Array Trigger** (ISU): Array trigger hardware, SFP transceivers, trigger logic.
  - Participants: ISU, ANL, UCLA
- **SP7 Central DAQ** (SLAC?): Telescope switches, central switches for data “crossbar”,client computer clusters for event building and harvesting, data reduction, quicklook, data storage system, data base.
  - Participants: SLAC, UCSC, WU, UMin
- **SP8 Calibration** (TBD): Calibration system for flat-fielding camera, single-pe measurements, absolute pointing calibration
  - Participants: Columbia, Barnard, UU, UD, IU
- **SP9 Optical monitor** (UU): Central pixel and electronics for intensity interferometry, optical pulsar timing, absolute pointing.
  - Participants: UU, UD

Camera Hierarchy



Camera Block Diagram



SP1 Photodectors	UCSC
SP2 FEE	SLACC
SP3 Backplane	Washington University
SP5 Camera Mechanical	UC
SP6 Array Trigger	ARGONNE/ISU
SP7 Central DACQ	TBD

Nomenclature

I suggest we agree on freezing some nomenclature to aid in discussions

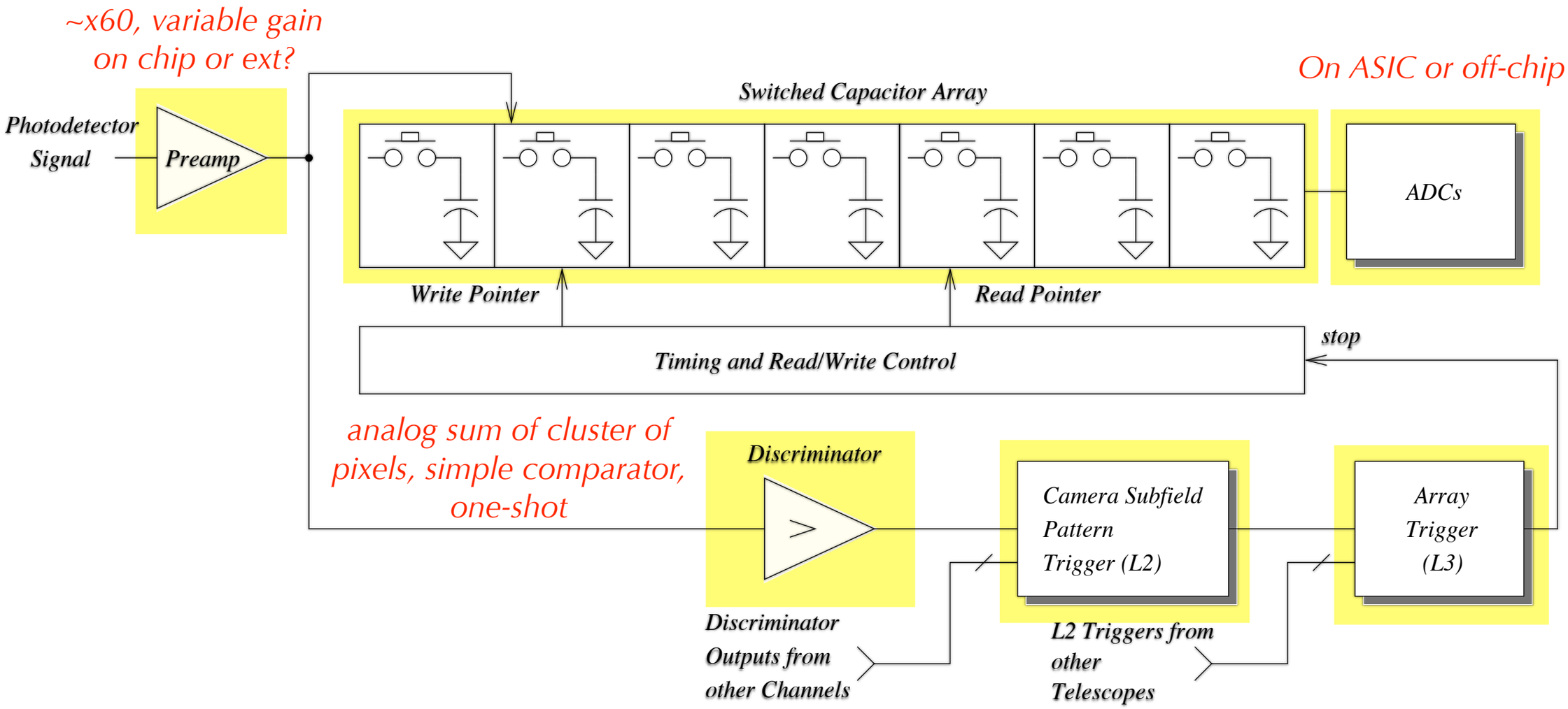
- **Photodetector Module** - 2″ MAPMT or 2″x2″ SiPM module
- **Camera Module** - 2″x2″ photodetector and front end electronics
- **Front End Electronics (FEE)** - stackup of TARGET ASIC boards behind PMT
- **Backplane** - Stackup of boards including 10″x10″ motherboard, and L2 and Backplane CPU mezzanie boards
- **Camera Subfield** - Assembly of 25 camera modules covering a field of view and one backplane *(VOTE: Subfield or Subsector?)*
- **Level 1 or Pixel Trigger** - Analog sum of 4 pixels + comparator and one-shot on FEE boards
- **Level 2 or Pattern Trigger** - Programmable logic on backplane FPGA that looks for, e.g., clusters of adjacent hits with 400 pixels. *(VOTE: L1.5 or L2...)*
- **Level 3 or Array Trigger -** Trigger at each telescope that makes delay matched coincidences with neighbors *(VOTE: L3 or L4?)*
- **Level 4 or Topological Trigger** - Trigger making use of high-level data (e.g. parallax) to refine the L3 trigger. *(VOTE: L3 or L4?)*
- **TACK** - Trigger returned from array trigger to FEE

Specifications

Primary Diameter	9m	7m
Number H8500 MAPMTs	177	177
Total number of pixels	11328	11328
Total number of L1 trigger pixels	2832	2832
Number of MAPMTs per subfield	25	25
FoV diameter	8.00	10.00
MAPMT size [mm]	52.0	52.0
Pixel angular size [deg]	0.06667	0.08333
Pixel angular size [arcmin]	4.00	5.00
Camera diameter [m]	0.78	0.78
Focal plane sag at FoV edge [mm]	-22.00	-27.00
PSF at FoV edge [arcmin]	3.81	5.65

Parameter	Nominal Spec.	Requirement	Rational
Total power	2kW	4kW	
Total weight		1 Ton	
Sampling Speed	1 Gsps	1 Gsps	SNR, Direct Cherenkov
Bandwidth	150 MHz	500 MHz	Nyquist
Sample time accuracy (relative)		1nsec	Direct Cherenkov
Analog Buffer Depth	16 usec	16 usec	deadtime reduction, hadronic rejection
Electronics Dynamic Range	10 bit		
Electronics resolution	9 ENOB		
Crosstalk		<1%	Image parameterization
Photodetector Dynamic Range		>1000 p.e.	
Photodetector Detection Efficiency	30% peak		
Single Photoelectron Resolution			
Optical Crosstalk		<1 %	Image parameterization
Electrical Crosstalk		<1%	Image parameterization
Gain		$>10^4$	
Pixel to pixel gain variations		<2	
L1 Trigger rate		>50 MHz rnd	
L2 Trigger rate	10-100 kHz	>1MHz	high density array/high scope multiplicity
L3 Trigger rate	5 kHz	>10 kHz	
Backplane data rate	100 MB/sec		(with x10 compression)
Peak telescope data rate	720 MB/sec		(10kHz with x10 compression)
36 telescope data rate	3.6 GB/sec, 150 TB/night		(assuming 5 scopes per trigger)

Electronics Approach

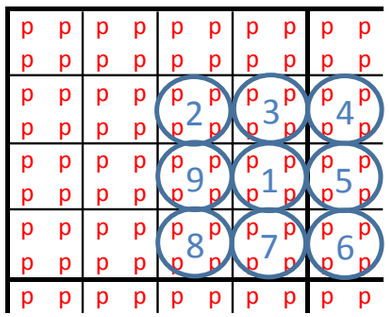


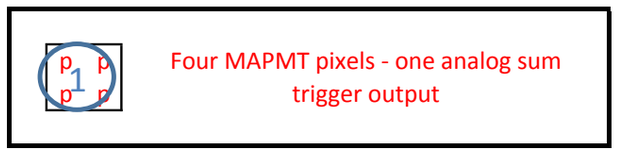
- Common stop on array trigger and very deep memory simplify design (no intermediate buffers, fast clear etc.), minimize deadtime, allows analysis of non-triggering scopes

- But how deep is deep enough? Local subclusters of telescopes? Is a common stop necessary, or is 30kHz telescope rate sufficient? Are untriggering telescopes important?

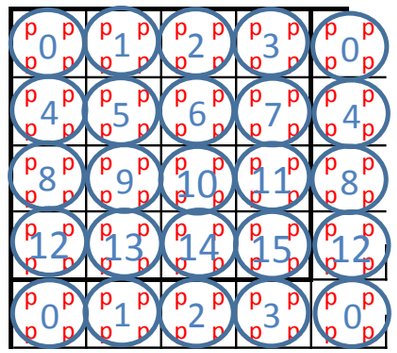
Pattern Trigger Logic

Example Cluster Logic



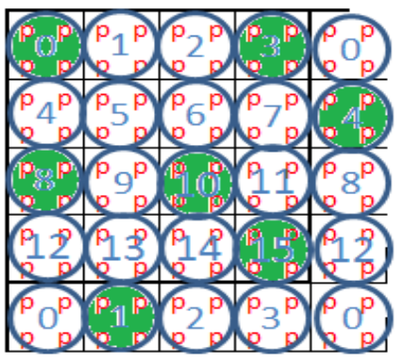


BackplaneTriggerSegment

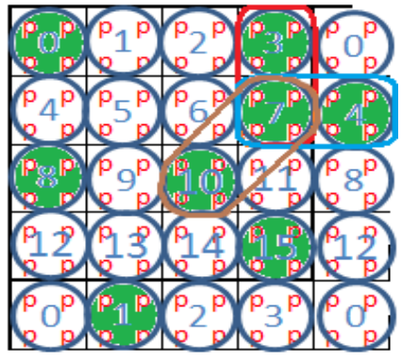


L2tr(BCK1Pxlxy11) := x(1) and
((x(2) and x(3)) or (x(2) and x(4)) or (x(2) and x(5)) or (x(2) and x(6)) or (x(2) and x(7)) or (x(2) and x(8)) or (x(2) and x(9))
or (x(3) and x(4)) or (x(3) and x(5)) or (x(3) and x(6)) or (x(3) and x(7)) or (x(3) and x(8)) or (x(3) and x(9))
or (x(4) and x(5)) or (x(4) and x(6)) or (x(4) and x(7)) or (x(4) and x(8)) or (x(4) and x(9))
or (x(5) and x(6)) or (x(5) and x(7)) or (x(5) and x(8)) or (x(5) and x(9))
or (x(6) and x(7)) or (x(6) and x(8)) or (x(6) and x(9))
or (x(7) and x(8)) or (x(7) and x(9))
or (x(8) and x(9)));

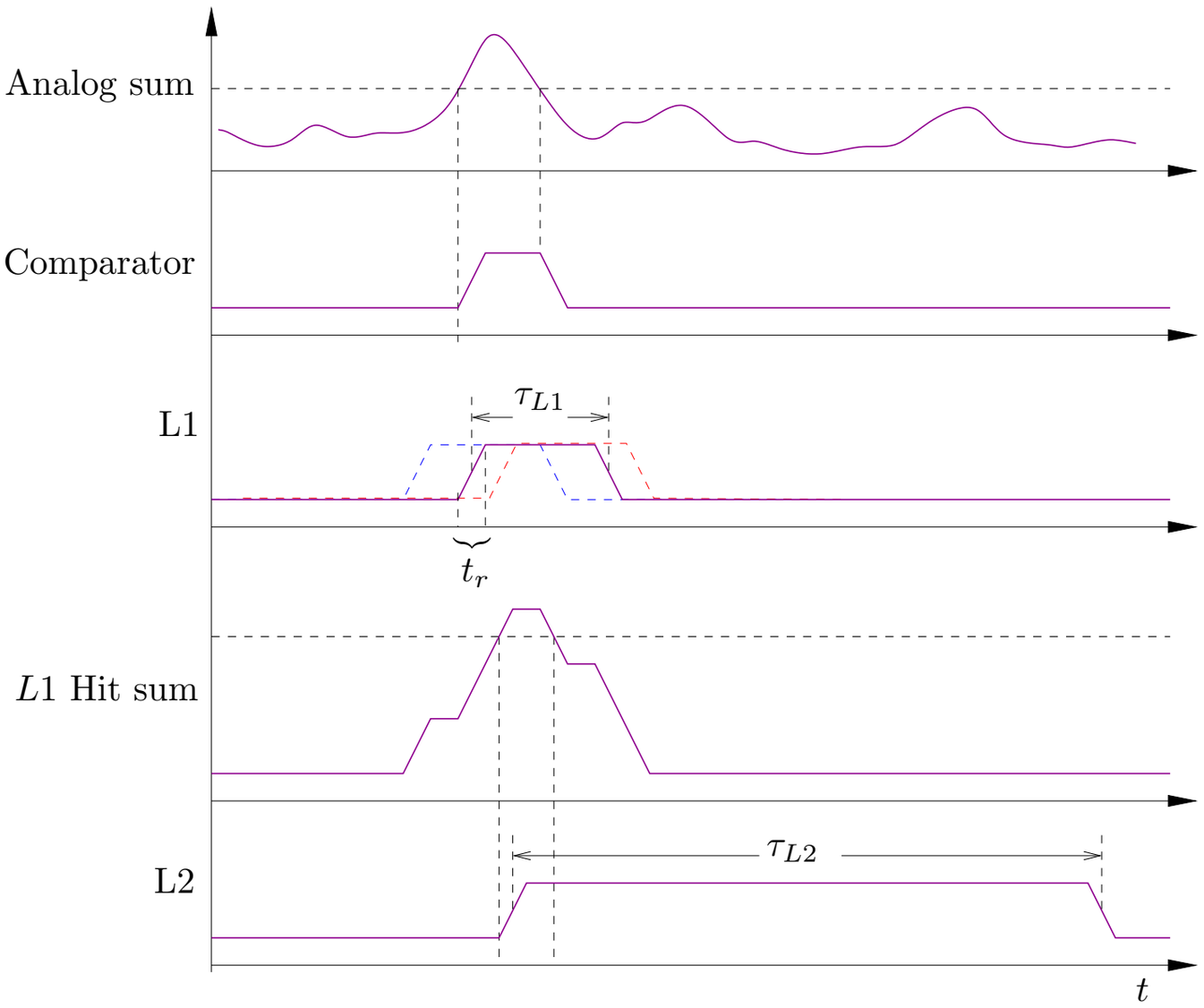
No Trigger



Trigger



Baseline Trigger Scheme



- Analog sum of (non-overlapping) groups of 4 pixels => 0.1 to 0.14 degree pixels for trigger (could be clipped for afterpulsing suppression)
- Simple comparator applied to analog sum gives L1 trigger
- Asynchronous combinatorial logic with matched delays forms L2 trigger (e.g., 3 adjacent hits from 400 channel inputs)

ICD Work

- Preparing ICDs between SCT camera components.
- At the level of engineers communicating about details.
- As an example, to the right we show a table from the SP 2-3 ICD (FEE and backplane) with the connector part numbers, pin-outs, signal levels, and description.
- Other ICDs (e.g. between the MAPTs and FEE subprojects as well as the Backplane and Mechanical design project) are currently under development.

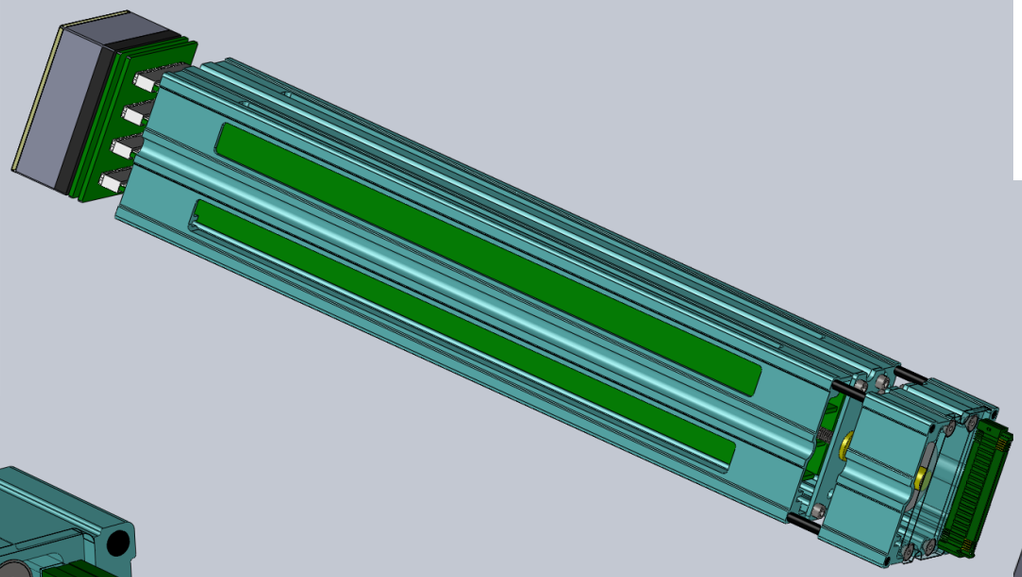
Backplane Connector	ERF8-040-05.0-L-DV-TR					
Camera Connector	ERM8-040-01-L-D-EM2-TR					
Row 0 #	**Signal**	**Description**	**Type**	**Row 1 #**	**Signal**	**Description**	**Type**
1	GND			2	GND		
3	Sync_p	Sync Marker TDB	LVDS	4	12V	Power	
5	Sync_n	Sync Marker TDB	LVDS	6	12V	Power	
7	GND			8	GND		
9	Trig_p	Trigger to FEE	LVDS	10	clk_p	125 Mhz Reference Clock	LVDS
11	Trig_n	Trigger to FEE	LVDS	12	clk_n	125 Mhz Reference Clock	LVDS
13	GND			14	GND		
15	Reset_p	Reset to FEE	LVDS	16	TrigType_p	TBD	
17	Reset_n	Reset to FEE	LVDS	18	TrigType_n	TBD	
19	GND			20	GND		
21	camera_tx_p	HS serial data from FEE	MGT	22	camera_rx_p	HS serial data to FEE	MGT
23	camera_tx_n	HS serial data from FEE	MGT	24	camera_rx_n	HS serial data to FEE	MGT
25	GND			26	GND		
27	Spare0_p	TBD		28	Spare1_p	TBD (0 ohm to 5V Power)	
29	Spare0_n	TBD		30	Spare1_n	TBD (0 ohm to 5V Power)	
31	GND			32	GND		
33	Trig0_p	Trigger Pixel From FEE	LVDS	34	Trig1_p	Trigger Pixel From FEE	LVDS
35	Trig0_n	Trigger Pixel From FEE	LVDS	36	Trig1_n	Trigger Pixel From FEE	LVDS
37	GND			38	GND		
39	Trig2_p	Trigger Pixel From FEE	LVDS	40	Trig3_p	Trigger Pixel From FEE	LVDS
41	Trig2_n	Trigger Pixel From FEE	LVDS	42	Trig3_n	Trigger Pixel From FEE	LVDS
43	GND			44	GND		
45	Trig4_p	Trigger Pixel From FEE	LVDS	46	Trig5_p	Trigger Pixel From FEE	LVDS
47	Trig4_n	Trigger Pixel From FEE	LVDS	48	Trig5_n	Trigger Pixel From FEE	LVDS
49	GND			50	GND		
51	Trig6_p	Trigger Pixel From FEE	LVDS	52	Trig7_p	Trigger Pixel From FEE	LVDS
53	Trig6_n	Trigger Pixel From FEE	LVDS	54	Trig7_n	Trigger Pixel From FEE	LVDS
55	GND			56	GND		
57	Trig8_p	Trigger Pixel From FEE	LVDS	58	Trig9_p	Trigger Pixel From FEE	LVDS
59	Trig8_n	Trigger Pixel From FEE	LVDS	60	Trig9_n	Trigger Pixel From FEE	LVDS
61	GND			62	GND		
63	Trig10_p	Trigger Pixel From FEE	LVDS	64	Trig11_p	Trigger Pixel From FEE	LVDS
65	Trig10_n	Trigger Pixel From FEE	LVDS	66	Trig11_n	Trigger Pixel From FEE	LVDS
67	GND			68	GND		
69	Trig12_p	Trigger Pixel From FEE	LVDS	70	Trig13_p	Trigger Pixel From FEE	LVDS
71	Trig12_n	Trigger Pixel From FEE	LVDS	72	Trig13_n	Trigger Pixel From FEE	LVDS
73	GND			74	GND		
75	Trig14_p	Trigger Pixel From FEE	LVDS	76	Trig15_p	Trigger Pixel From FEE	LVDS
77	Trig14_n	Trigger Pixel From FEE	LVDS	78	Trig15_n	Trigger Pixel From FEE	LVDS
79	GND			80	GND		

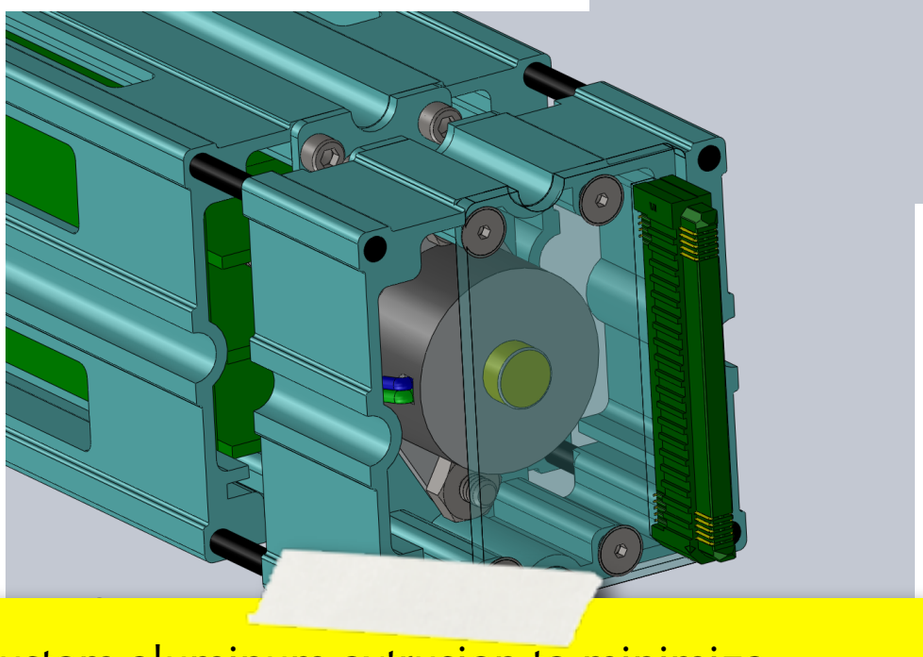
Cost

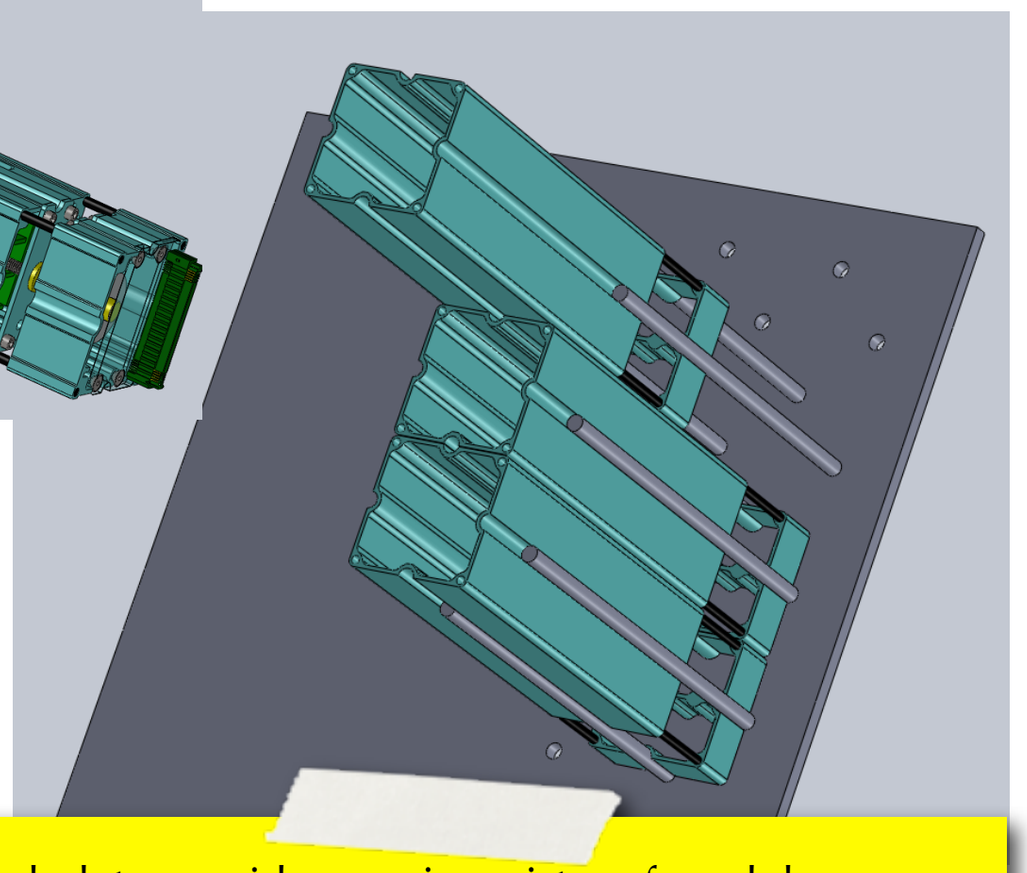
- Use of TARGET ASICs (incorporating deep analog pipeline and A/D conversion) allow huge reduction in cost per channel compared, e.g., to baseline CTA approaches (NeCTAR, FlashCam)
- Footnote: Incorporating discriminator logic may increase number of design iterations and risk, without a huge impact on cost (as shown below)

Item	13,000 channels		640,000 channels	
	Unit price	Cost/ch	Unit price	Cost/ch
ASIC	**$65**	**$4.06**	**$15**	**$0.94**
External variable gain amps and discrim.		$2.75		$2.75
FPGA (XC5VLX30T)	$235	$3.67	$176	$2.75
HV module	$140 ($40)	$2.19 ($0.62)	$105	$1.64
Connectors		$1.17		$0.88
FPGA board components		$2.42		$1.82
PS board components		$1.14		$0.85
PCB fabrication	**$9~38**	**$1.70**	**$5~22**	**$0.91**
Board stuffing	$10~40	$2.44	$8~30	$1.76
Module mechanical components (1 hr/mod)		$0.625		$0.625
Hand assembly and testing (1hr/mod)		$0.625		$0.625
Total: Assuming on-chip trigger/preamp		**$19.95**		**$12.79**
Total: Assuming external amp and disc.		**$22.70**		**$15.54**
Total: External amp, disc and new HV		**$21.13**		**$14.52**

WU Strawman Design







Custom aluminum extrusion to minimize mechanical costs.

Adjustable distance between backplane plate and PMT windows.

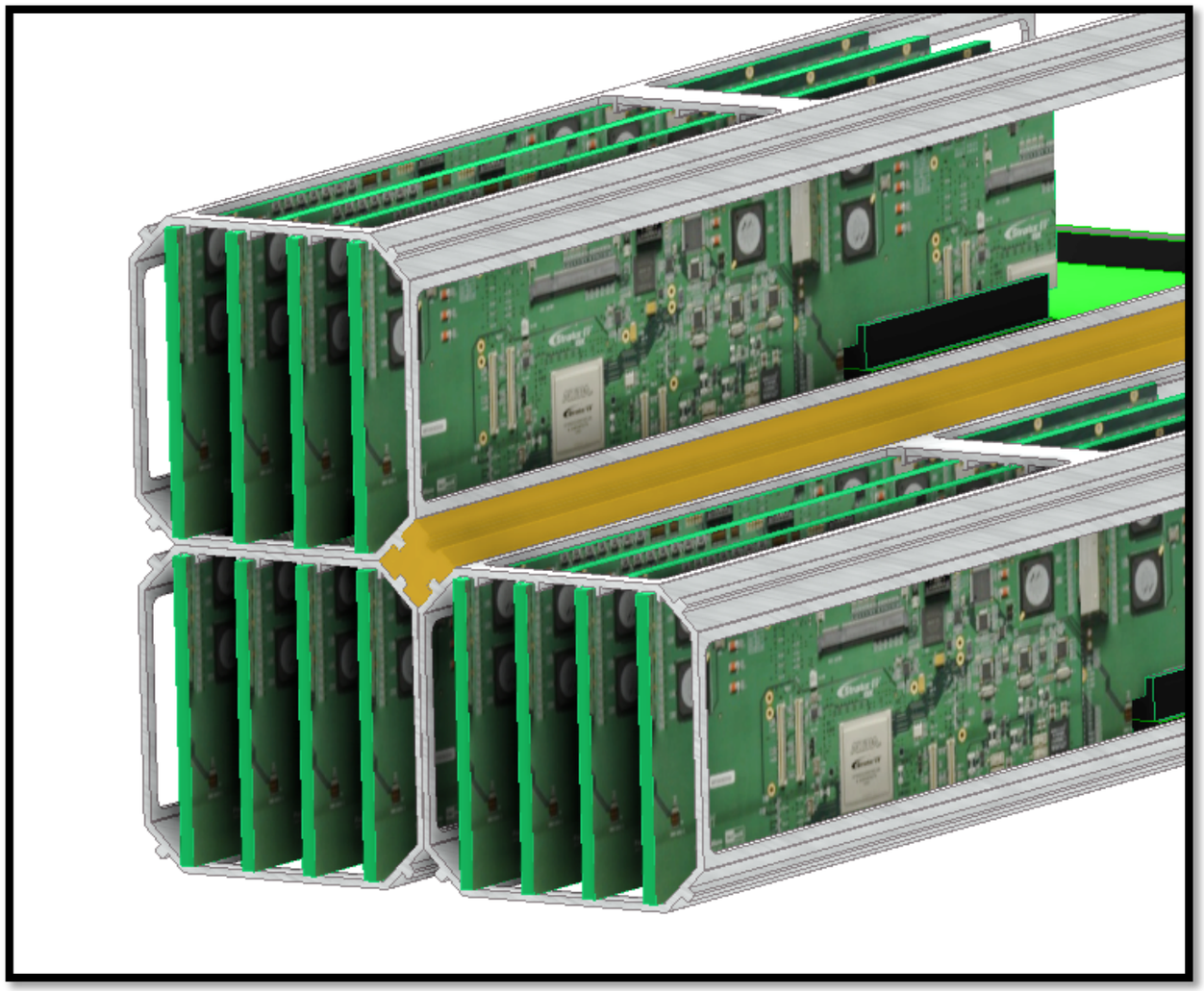
Back of module pulled against plate (pushed out) with a single screw through backplane

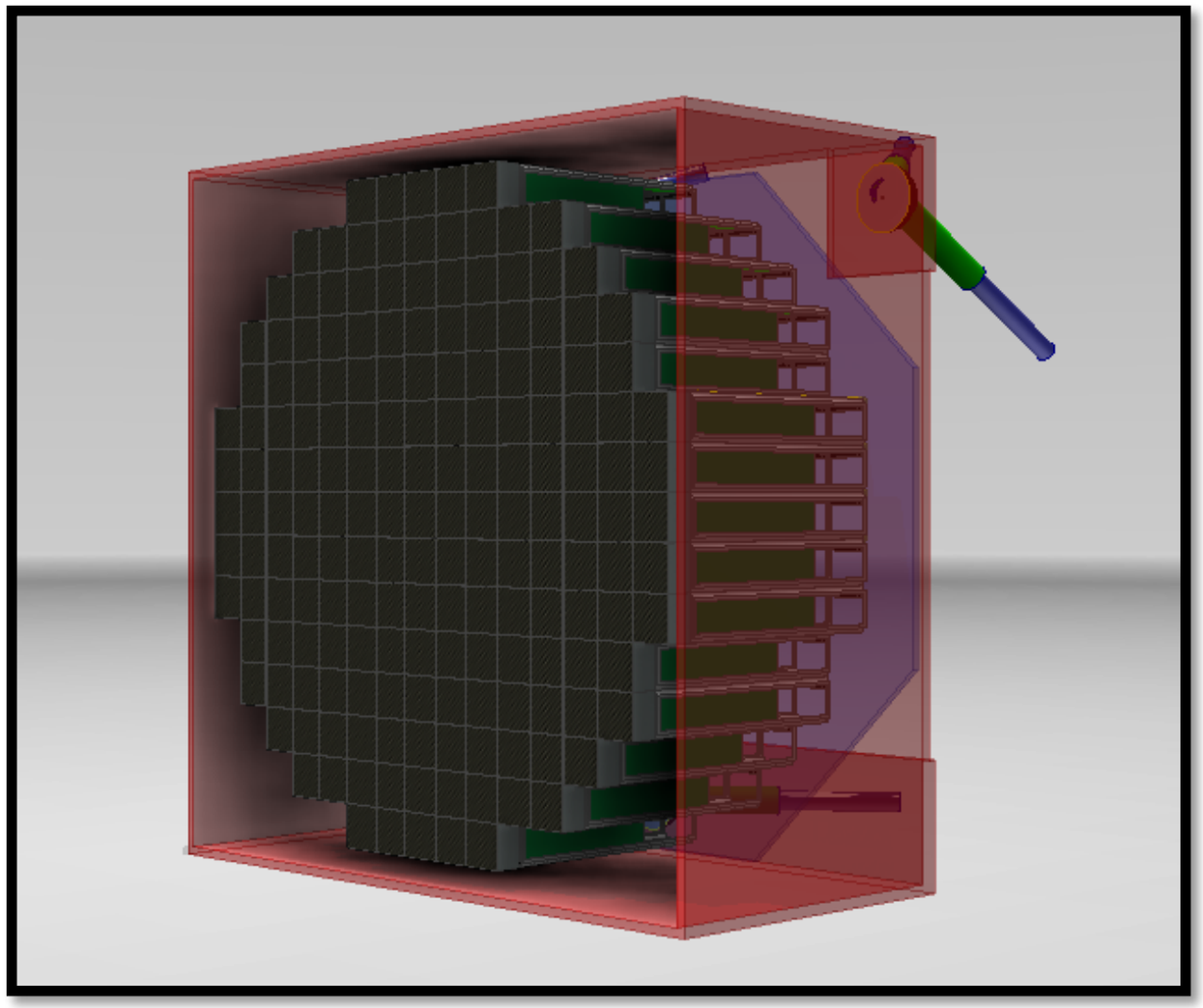
Tool plate provides z-axis registry of modules

Posts provide alighnment in x-y plane and rigidity with minimal inter-module deadspace

Electronic backplane monts to back of tool plate. Modules removed from front after loosing screw through backplane.

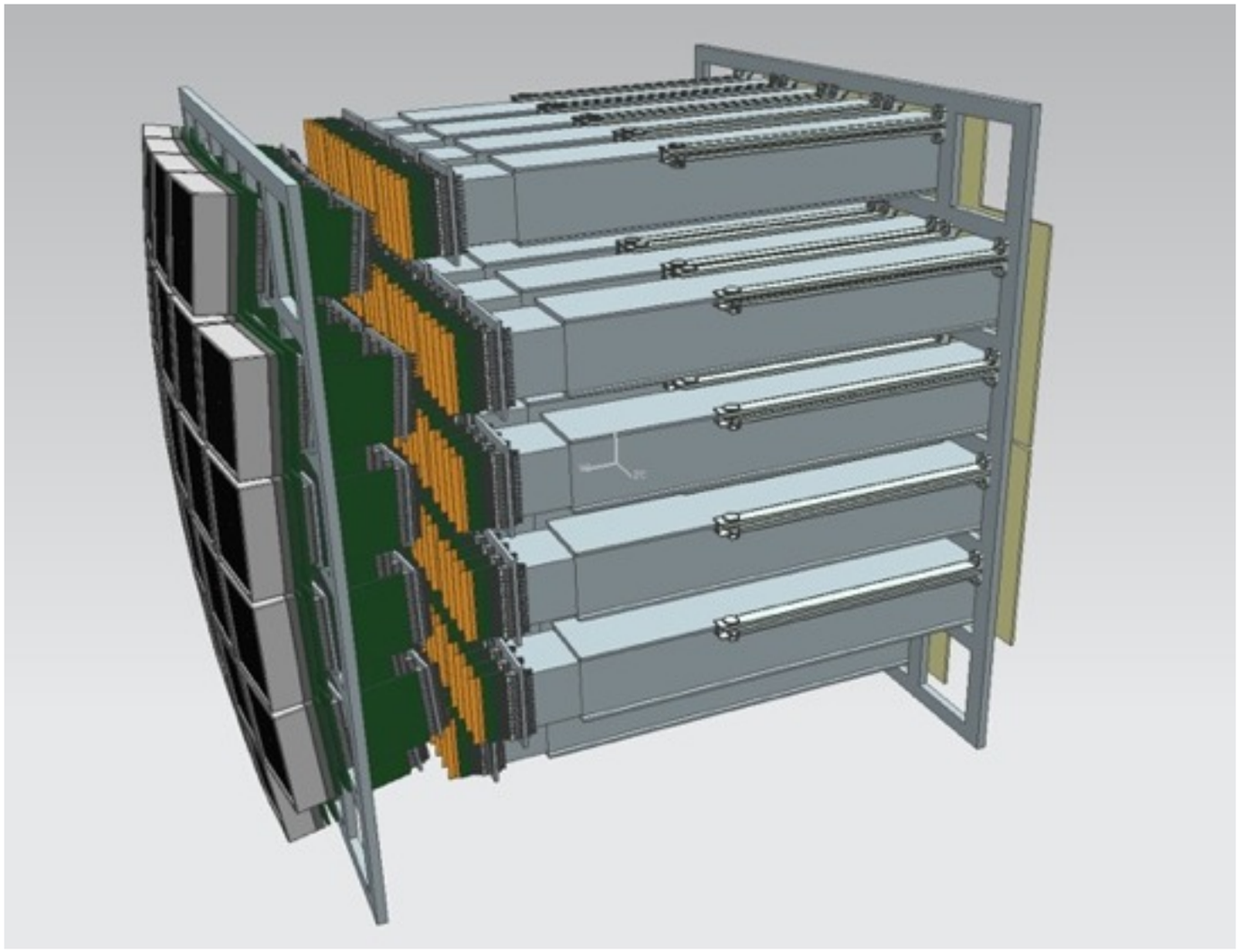
Camera Mechanics





- Scott presented UC design - Backplate and guideposts might provide a good way of conducting heat out of the Peltier coolers for the SiPMs

SST/MST SC Collaboration

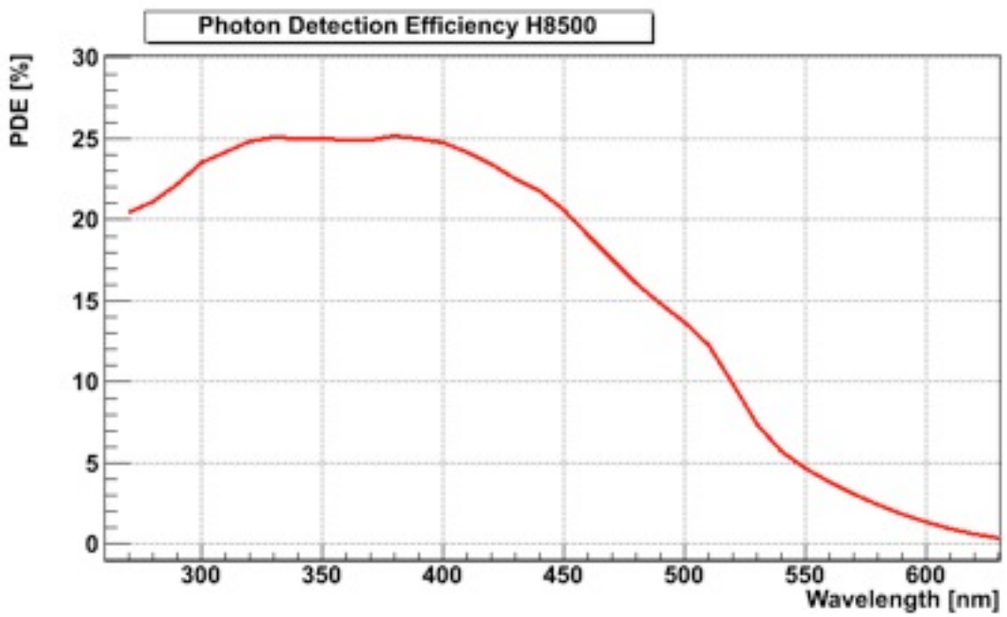


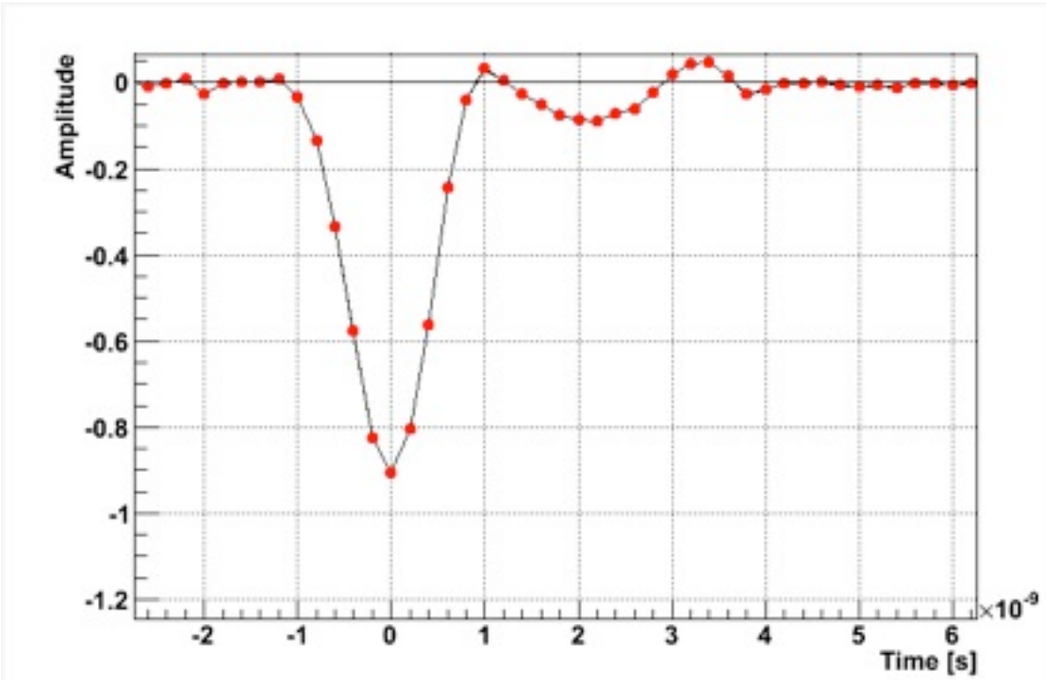
- SLAC and WU groups working with UK SST group to provide FEE and backplane electronics.

- Could explore other areas that would benefit from common development

MAPMTs

Model	Hamamatsu R8500	
Cost	~$2k	☺
Number of pixels	64	
Dimensions	52mm x 52mm	
Gain	12 stage 1.5 x 10^6	
Peak Cathode QE	~35%	☺
Charge collection Eff	~70%	☹
Gain variations	15% RMS, x2 spread	☹
Variations with 4pixel clusters	20%	
Rise time	0.4nsec	☺
Time jitter/transit time spread	4nsec, 0.4nsec spread	☺





Discussion

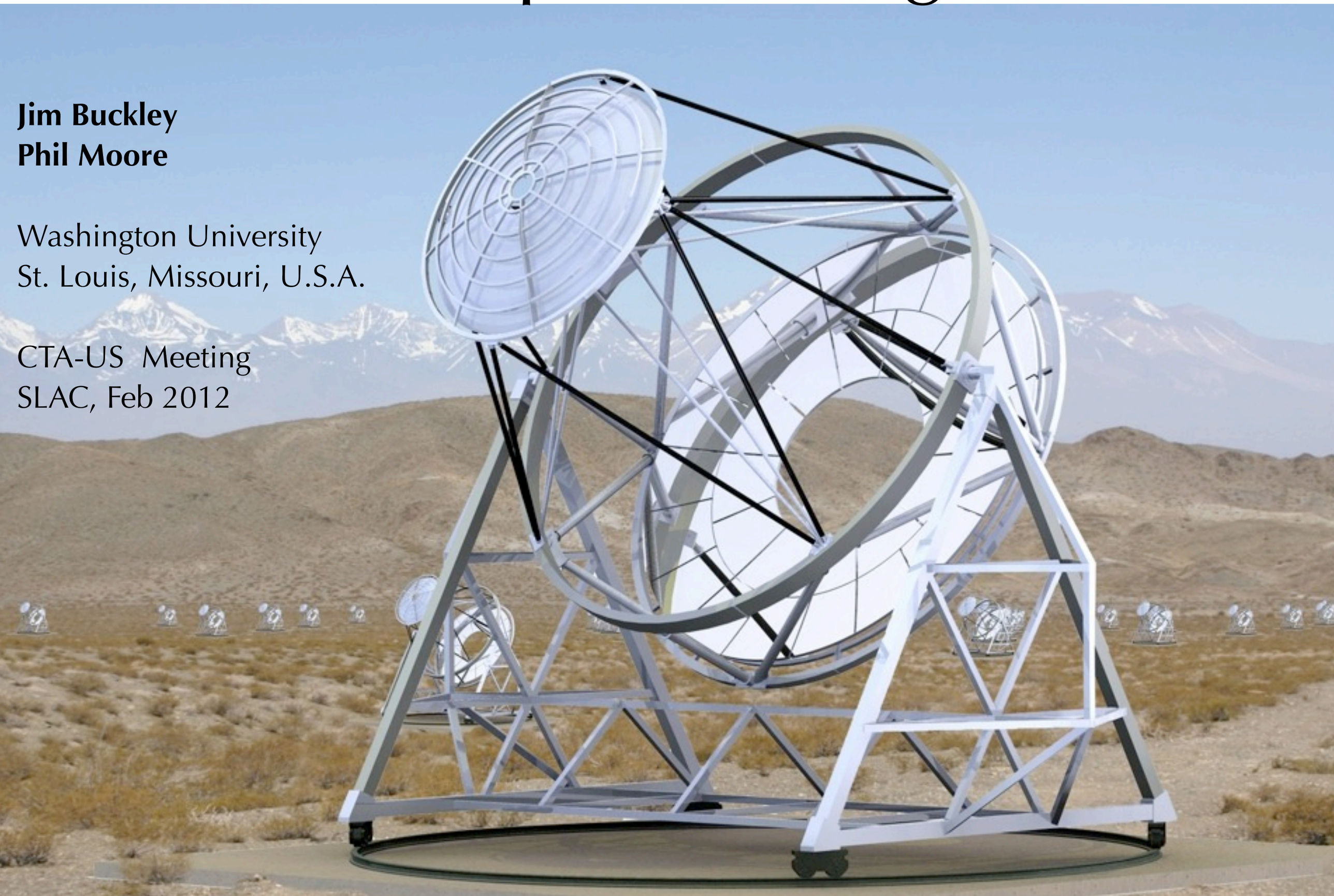
- Need to generate documentation - PTDR, Specs, ..
- Open questions
  - Impact of SiPMs
  - Common design for SiPMs and MAPMTs?
  - TARGET ASIC redesign
  - Trigger for FEE - ASICs?, on TARGET?, discrete components
  - Optimum trigger scheme from simulations
  - Other....

Backplane Design

Jim Buckley
Phil Moore

Washington University
St. Louis, Missouri, U.S.A.

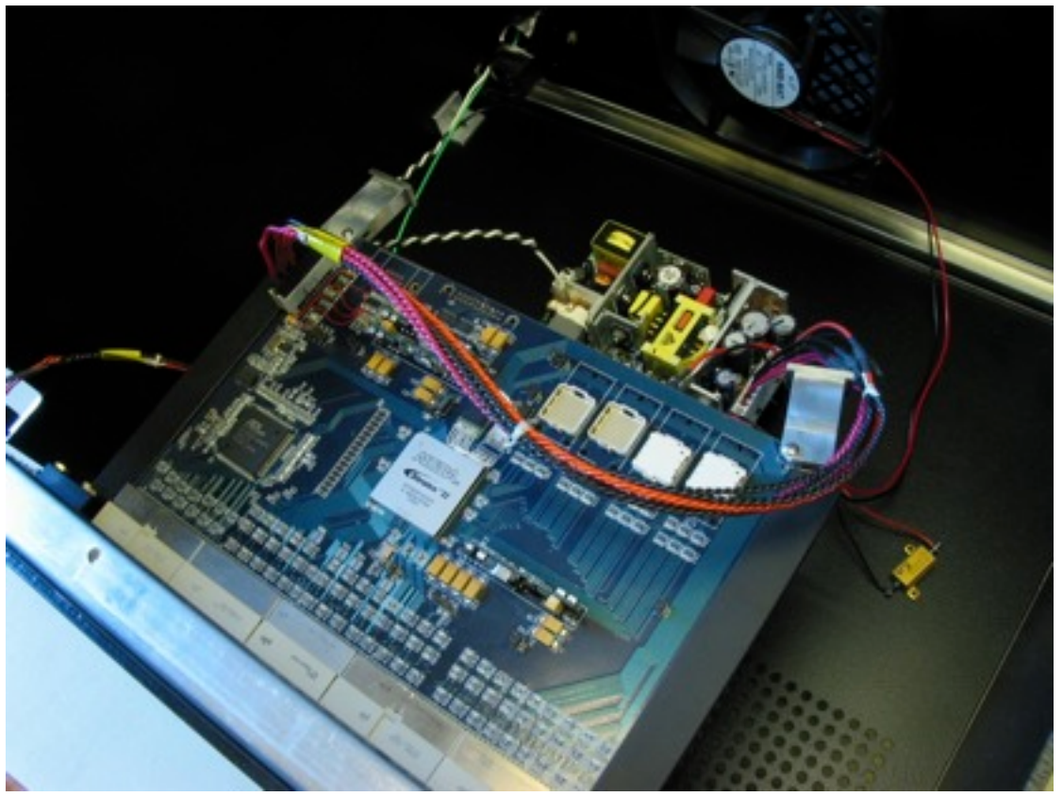
CTA-US Meeting
SLAC, Feb 2012



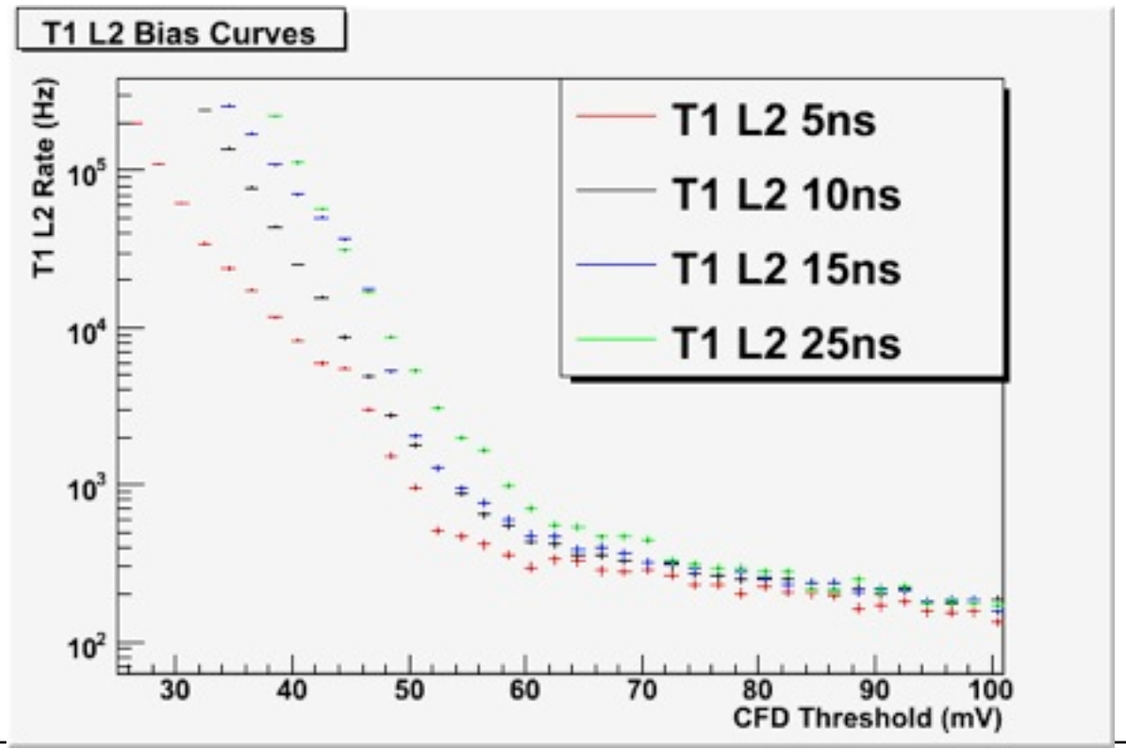
Backplane

- Partitioning of camera into subfields, allows trigger to be decomposed into non-overlapping regions (2.7deg size comparable to Gen-I ACT FoV).
- Modularity, high-level integration, elimination of cables (with controlled impedance traces) provides lower cost, better reliability, modularity for lower-cost development and easier maintenance.
- Primary functions of backplane:
  - DACQ - combining 25 serial data streams from FEE on each backplane, merging backplanes with 10GbE switch.
  - High speed data processing (VERTEX-6 and CPU) for event building and data compression.
  - 400 input pattern trigger (Spartan-6 for latching patterns, timing alignment and combinatorial logic).
  - Clock, TACK, Synch pulse distribution (phase locking, phase shifting, synchronization)
  - Power distribution, monitoring, sequencing

Backplane L2 Trigger



- In 2009, 500 channel system tested on VERITAS is a prototype for SC backplane with 400 pixels + 76 overlap pixels
- Use of simple combinatorial logic (with a VHDL code generator) get very short coincidence resolving time
- Cost of about $1k per subfield



DACQ Prototype

- Used Altera Protoboard, Altera's SOPC design automation tools, Altera 4-lane PCIe IP core
- Used Jungo driver development tool together with our own code to create a PCIe/DMA interface
- Sustained average transfer to/from memory on the CPU of 270 MB/sec (write) and 330 MB/sec read for a complete end-to-end test. With more lanes, better optimations several GB/sec (not Gb/sec!) should be possible.
- With a Wash U CSE programmer that developed a similar PCI-X driver, develop new custom driver to achieve >1 GB/sec *with source code*.

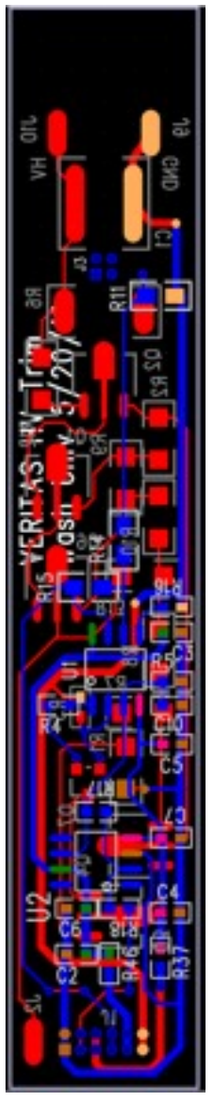
Status

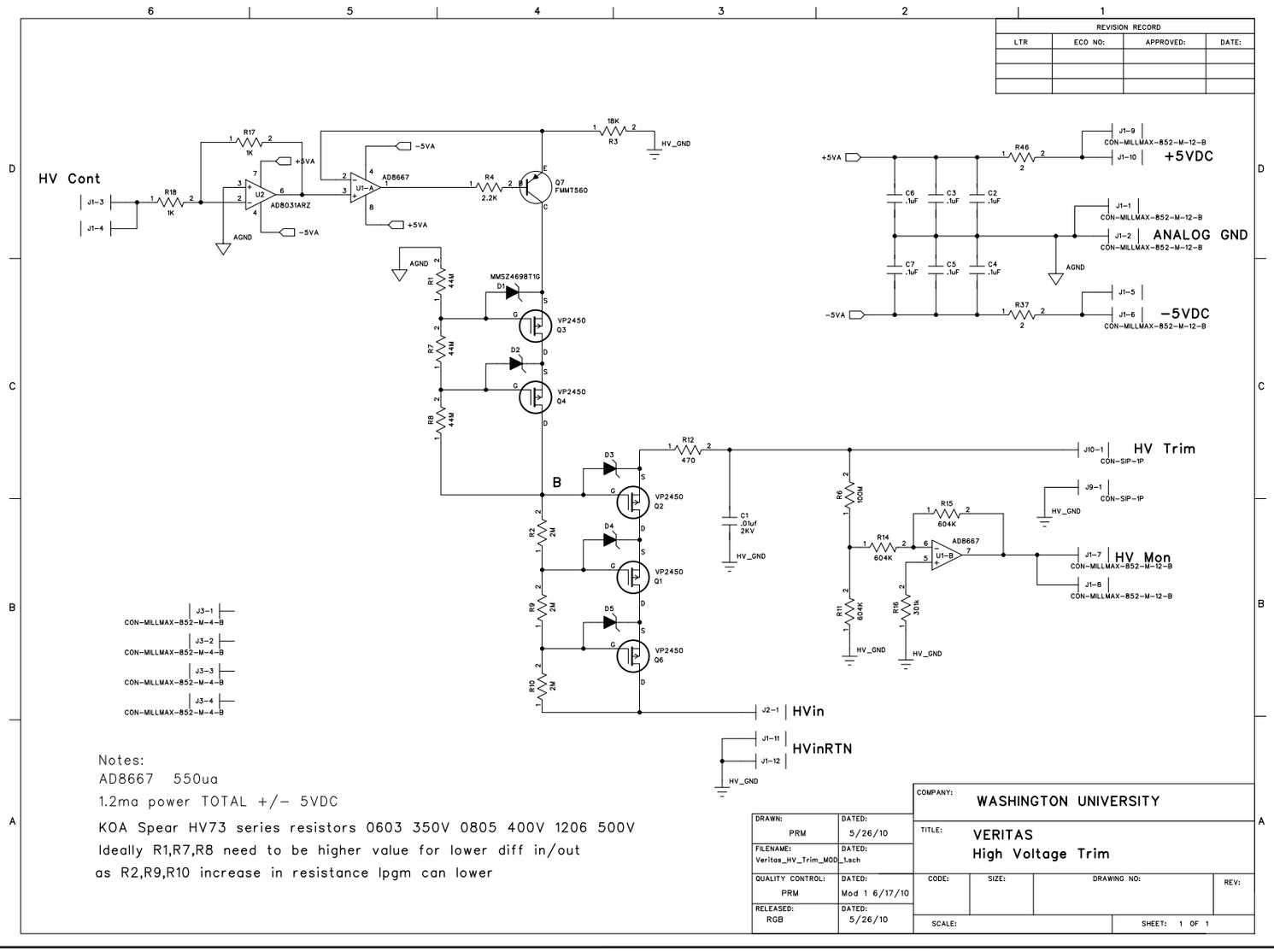
- No external funding
- Change in FPGA type (Altera to Xilinx)
- Development of new DMA engine and drivers by WU CSE group
- Developing ICDs, front end electronics simulator (beginning of test fixture)
- HDL development
- Schematic design of FPGA daughterboard and backplane

Parameter	Description	Detailed Specification	Nominal Value	Requirement
BP Dimensions	Width x Length x Height (including daughterboards and heat sinks, but not camera modules)		254mmx254 mmx114mm	< (260mm-drawer wall thickness)
BP Weight	Including daughterboards and heat sinks without mechanical drawer supports or camera modules		2 kg (est)	< 5 kg
BP daughterboard form factor	Form factor (dimensions) for mezzanine boards on FPGA including CPU and DACQ FPGA boards	PC104		
Backplane connector		ERF8-040-05.0-L-DV -TR		
Camera Module connector		ERM8-040-01-L-D-E M2-TR		
BP daughter board connectors	PCIe/104 stacking connector	QMS-078-06.75-L-D		
Backplane aggregate input data rate	Combined data rate from 25 serial data streams into the DACQ FPGA for processing		1 GB/sec average, 10 GB/sec burst	
Backplane DACQ FPGA data output	Sustained data rate over PC104 PCIe connector to backplane CPU	8-lane PCIe	4 GByte/sec	>102 MB/sec (1 GB/sec) with 10x (no) compression
Backplane CPU output data output		10GigE Ethernet	1 GByte/sec	>102 Mbytes/sec (1 GB/sec) with 10x (no) compression
Backplane DC Power Supply Voltage Level	Power supply used for backplane FPGAs, FEE/camera modules and backplane CPUs		12VDC	
Backplane DC Power Supply Current	Including 100W estimate for backplane and CPUs + 25x10W estimate for camera modules		350 W	475 W
Programming Interface	DACQ and TRIG FPGA HDL programming interface	JTAG and PCIe from Crate Computer		
DACQ FPGA	FPGA on BP daughterboard used for merging and processing highspeed serial data from camera modules, and command interface	Vertex 6 XC6VHX250T-3FFG 1154C		
L2TRIG FPGA	FPGA on BP for finding patterns of hits in 400 pixel trigger signals from camera modules	Spartan 6 XC6SLX100T-3FFG900		
L2TRIG Coincidence Resolving Time			4nsec to 20nsec programmab le	Minimum of 4nsec
L2TRIG Input Singles Rate			40 MHz	Maximum 100MHz
L2TRIG Input Time Alignment			1 nsec	<2 nsec for single p.e. pulses
L2TRIG Output Trigger Rate			100 kHz	Maximum 10 MHz
L2TRIG Output Format	Leading edge time followed by latched hit pattern	3Gbps serial???		

HV Trim Circuit

- WU group completed prototype of HV system based on linear HV trim circuit, very low ripple precise linear control - could be used with DC MST or LST cameras.
- Together with built in voltage, current monitor and ACTEL FPGA provides fast shutdown based on local logic (no communication links).





HV Description

The High Voltage Trim circuit works by reducing the incoming high voltage power supply by a programmable amount. There are four building blocks that make up the circuit as depicted below. The constant current control (green block), voltage compliance (pink block), voltage follower (blue block), and output monitor (red block). The amount of voltage reduction is determined by the constant current control circuit. An input voltage Vin establishes the constant current at a value of I as set by R3/Vin. This current is determines the voltage drop across the string of R2 +R9+ R10. P channel MOSFETs Q1, Q2 and Q6 act as voltage followers, with the Source of each device equal to the voltage at the Gate of the device minus approximately 5V. The VP2450 are 500V Mosfets and the FMMT560 is a 500V PNP transistor. To control negative1450V and to not exceed the 500 voltage ratings of those devices, a chain of three devices in series to drop voltage equally was devised. To increase the compliance voltage of the programmable current source, R1, R7, R8, Q3 and Q4 equally divide the program current value by one third. R6, R11, R14, R15, R16 and U1-B make up the High Trim Voltage Monitor circuit with the output equal to 333.2 Volts per volt.

Amplifier U1-A, R4, R3 and Q7 comprise the control portion of the circuit, a 0uA to 240uA programmable constant current sink. U2 acts as a unity gain inverting amplifier to present a negative voltage of the same value as J1-3 to amplifier U1-A. U1-A will bias Q7 base current in to a value to set the voltage developed at the R3 Q7 Emitter to equal the input voltage of U1-A. Consequently the R3 current value is equal to the input voltage at J1-3 divided by the value of R3, 18K ohms. The programmed Trim Voltage Output is determined as follows:

Desired Trim Voltage Drop (Vdrop) = HV in – TrimV_out + 5 (Q2 Vgs)
drop_current = Vdrop/6e6;
error current = TrimV_out/132e6 (R1, R6, R7 bias current error)
pgm_current = drop_current - error_current;
J1-3_voltage = pgm_current * 18000.0;